REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on December 22, 2000, and the reference cited therewith.

Claims 20, 21, 23-29, and 33-35 are amended, and claims 37-40 are added; as a result, claims 17 - 40 are now pending in this application. Claims 37-40 are based on subject matter present in the specification; no new matter has been added.

Information Disclosure Statements

The foreign and non-patent publications cited in the Information Disclosure Statement were not considered in this Office Action since they were not provided by the applicant and were not in the file wrapper of the parent application.

Enclosed is a copy of Patent No. 6,025,225, which is the parent of the above identified application. Please note that all of the references cited in the Information Disclosure Statement filed in the present application on December 20, 1999 are listed in the issued patent. Applicant respectfully asserts that copies of these references do not need to be provided as they were cited and considered in the parent application.

Applicant respectfully requests that an initialed copy of the 1449 Form, listing all the all references that were submitted with the Information Disclosure Statement filed on December 20, 1999, marked as being considered and initialed by the Examiner, be returned with the next official communication.

Objection to the Specification

The disclosure is objected to because element 111 was incorrectly identified as 104. The specification has been amended to correctly identify element 111.

Rejection Under 35 U.S.C. § 112

In the Office Action, claims 25, 29 and 30 were rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 25 and 29 have been amended to correct the lack of antecedent basis. Accordingly, Applicant respectfully traverses this rejection.

Rejections Under 35 U.S.C. § 103

In the Office Action, claims 17 - 36 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Wen (U.S. Patent No. 5,191,509). Applicant respectfully traverses this rejection, as discussed below.

Claims 17-25 and 31-34 are directed to a memory cell formed in a layer of semiconductor material outwardly from a substrate. Claims 26-30, 35 and 36 are directed to a memory devices including the memory cells of Applicant's invention.

Wen teaches forming a trench storage capacitor directly in a substrate. Wen, Col. 3, lines 14-16. Forming the trench storage capacitor of Wen directly in the substrate requires that a layer of hemispherical grain *doped* polysilicon be deposited on the wall of the trench in forming the electrode (114). Wen, Col. 4, lines 13-23. The deposited layer of hemispherical grain doped polysilicon is then etched to achieve a textured surface. Wen, col. 4, lines 19-26.

Examiner cites the Forbes reference (U.S. Patent No. 5,909,618), the Pfiester reference (U.S. Patent No. 4,761,452) and the Wahlstrom reference (U.S. Patent No. 5,396,452) (collectively, "the Cited References") as art that shows it is well known that (a) capacitor plates are inherently connected to source/drain regions of peripheral transistors, and (b) bit and word lines are coupled to source/drain regions and gates of access transistors along with a column decoder and row decoder to access the cells of an array. The obviousness rejection is based on Wen in light of knowledge in the art as reflected in the Cited References.

A prima facie finding of obviousness requires a showing that (a) all the claim limitations in the rejected claim are present in the references cited, (b) there is motivation to combine the references, *and* (c) there is a reasonable expectation of success in combining the references.

Applicant's claimed invention cannot be formed simply by directly combining Wen with any or all of the Cited References. If such combination were made, the resulting memory device/memory array would not be functional. This is because Wen simply teaches how to form a trench capacitor directly in a substrate. Wen provides no instruction as to how the trench would actually be used to form a memory device or memory array, particularly one that is formed substantially *atop* the substrate. Applicant's invention is directed to a memory device or a memory array and involves forming a transistor with a first source/drain, a body region and a second source drain in combination with a trench capacitor, all formed *atop* the substrate.

In particular, Wen teaches the use of doped polysilicon to line the interior of the trench. Col. 4, lines 13-18. The doped polysilicon is then etched with an etchant that, by definition, attacks doped polysilicon, to form an electrode with a textured surface.

Applicant's claimed invention involves forming a transistor structure atop and adjacent a trench. In Applicant's invention, the transistor structure must be protected (masked) during the formation of the doped polysilicon electrode in the trench, and then the mask removed. Note that the transistor structure in Applicant's claimed invention includes a doped first source/drain region, a doped body region, and a doped second source/drain region.

Following the teaching of Wen and the Cited References, the formation of a memory device or array would involve using *doped* polysilicon to line the trench (including the sides of the transistor device) and then etching this lining to form the textured electrode. However, the portion of this layer covering the transistor device would have to be selectively removed. This is problematic because the material covering the transistor and the material forming the electrode are one in the same. On the other hand, if the transistor portion is not masked, the texturizing etch would attack the transistor structure because it is also formed from doped polysilicon. This would render the device non-functional.

Clearly, the fabrication of a memory device having structure formed above the trench is a more complicated process than simply forming a trench ala Wen and adding the structures disclosed in the Cited References. Wen falls far short of providing the necessary motivation or

guidance to one skilled in the art of how to combine the trench structure taught therein with other structures, such as those disclosed in the cited references, to fabricate a memory device or memory cell.

As Applicant has discovered, the formation of a memory device or memory array requires the unobvious step of depositing *undoped* amorphous polysilicon on the walls of the trench, including on the sides of the transistor device. Page 9, lines 3-4. The portion of the undoped polysilicon layer covering the sides of the transistor device serves as a protective layer (mask) that does not interact with (e.g., diffuse dopants into) the various doped regions making up the transistor structure. The entire structure is then heated so that dopants diffuse from the first source/drain into the portion of the amorphous silicon layer surrounding the first source/drain. The heating is performed such that dopants do not diffuse out of the transistor structure. This results in the formation of a doped silicon layer immediately adjacent the first source/drain region that has the same dopant type as the first source/drain region. Page 9, lines 3-6. This doped silicon layer serves as a plate (electrode) for the trench capacitor. The use of an *undoped* amorphous silicon layer to line the trench enables the use of an etchant that preferentially attacks the *undoped* remaining portion of the polysilicon trench layer serving as the mask for the transistor structure (FIG. 3). Use of doped polysilicon, as called for in Wen, requires the use of an etchant that attacks doped polysilicon. This would result in the removal of both the mask *and* the newly formed doped polysilicon layer, thereby rendering the device non-functional.

In light of the above, Applicant respectfully traverse the rejection of claims 17-36 and believe these claims to be patentable. Accordingly, Applicant respectfully request that the rejection to claims 17-36 be withdrawn.

Product-by-Process Limitations

Examiner has included in the Office Action a reminder pertaining to "product by process" limitations drawn to a structure. In particular, Examiner notes that limitations that do not offer structural variation to the final product are given no patentable weight.

Applicant has amended claims 20, 21, 23, 24, 27, 28, 33-35 to more particularly point out the structural variation to the final device, rather than the process steps by which the limitation is achieved. Accordingly, Applicant submits that the aforementioned claims, as amended, include structural limitations that have patentable weight. In particular, it is submitted that an anodic-etch-roughened surface and a phosphoric-etch-roughened surface are different structural limitations to a surface.

CONCLUSION

Claims 20, 21, 23-29 and 33-35 are amended herein. Claims 37-40 are added hereby. Claims 17- 40 are now pending.

Applicant believes all the claims are in condition for allowance and requests reconsideration of the application and allowance of the claims. Please charge any fees deemed necessary to Deposit Account 19-0743. The Examiner is invited to telephone the below-signed attorney at 612-373-6913 to discuss any questions which may remain with respect to the present application.

Respectfully submitted,

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By their Representatives,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 22nd day of March, 2001.

Amy Moriarty
Name

Amy Moriarty
Signature

Marked-Up Version of the Amended Paragraph

Word line 112 passes body region 108 of access transistor 111 in isolation trench 114. Word line 112 is separated from body region 108 of access transistor [104]111 by gate oxide 116 such that the portion of word line 112 adjacent to body region 108 operates as a gate for access transistor 111. Word line 112 may comprise, for example, N+ poly-silicon material that is deposited in isolation trench 114. Cell 102D is coupled in a column with cell 102A by bit line 118.